



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,899	09/23/2003	Akiharu Miyanaga	07977-254003 / US3823D1D1	8644
26171	7590	07/22/2008		
FISH & RICHARDSON P.C. P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			EXAMINER	
			VU, DAVID	
			ART UNIT	PAPER NUMBER
			2818	
MAIL DATE	DELIVERY MODE			
07/22/2008	PAPER			

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/667,899	MIYANAGA ET AL.
Examiner	Art Unit	
DAVID VU	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 17 March 2008.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 39-61 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 43-49 is/are allowed.

6) Claim(s) 39-42 and 50-61 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 23 September 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

- 1) Certified copies of the priority documents have been received.
- 2) Certified copies of the priority documents have been received in Application No. 09/246014.
- 3) Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date _____

5) Notice of Informal Patent Application

6) Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 39, 50, 59 and 60 are rejected under 35 U. S. C. 102(b) as being anticipated by Shimizu et al. (US Pat. 5,217,910, hereinafter Shimizu).

Regarding claims 39 and 59, Shimizu discloses in figs. 9E a semiconductor device comprising:

a.semiconductor substrate 21;

a channel region formed in semiconductor substrate 21; wherein channel region is located between source and drain regions p;

at least first and second impurity regions 37 formed in channel region wherein first impurity region 37 (on the left side of the gate) is in contact with source region p and second impurity region 37 (on the right side of the gate) is in contact with the drain region p; first and second impurity regions 37 (n-type) are doped with an impurity of a conductivity type opposite to source and drain regions (p-type); wherein first (left side) and second (right side) impurity regions are separated from each other.

at least third and fourth impurity regions 31 (n⁻-doped regions) formed in semiconductor substrate wherein third and fourth impurity regions 31 are **electrically** in contact with the

source/drain regions (p-doped regions) and are separated from each other and wherein a conductivity type of third and fourth impurity regions (n-type) are opposite to that of source and drain regions (p-type)

a gate insulating film formed over the channel region; and

a gate electrode 28 over the channel region with the gate insulating film interposed therebetween, wherein first (left side) and second (right side) impurity regions are separated from each other.

Regarding claim 50, Shimizu discloses in figs. 9E a semiconductor device comprising:
a semiconductor substrate 21;
a channel region formed in semiconductor substrate 21; wherein channel region is located between p-source and p-drain regions;
at least first and second impurity regions 31 formed in channel region wherein first impurity region 31 (on the left side of the gate) is **electrically** in contact with the p-source region (left p-region) and second impurity region 31 (on the right side of the gate) is **electrically** in contact with the p-drain region (right p-region); first and second impurity regions 31 (n-type) are doped with an impurity of a conductivity type opposite to source and drain regions (p-type); wherein first (left side) and second (right side) impurity regions are separated from each other; in other word, the first and second impurity regions 31 are in contact with the same pair of p-source/drain.

at least third and fourth impurity regions 37 (n⁻-doped regions) formed in semiconductor substrate wherein third impurity regions 37 (right n-region 37) are **electrically** in contact with

the drain regions (right p-region) and fourth impurity regions 37 (left n-region 37) are electrically in contact with the source regions (left p-region)

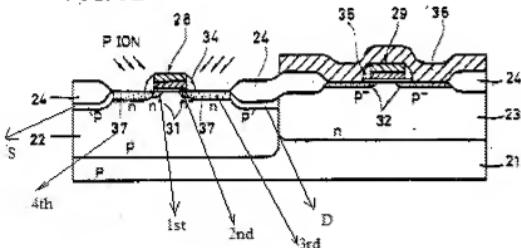
a gate insulating film formed over the channel region; and

a gate electrode 28 over the channel region with the gate insulating, film interposed therebetween, wherein first (left side) and second (right side) impurity regions are separated from each other; and wherein first and second impurity regions 31 are overlapped by gate electrode at least partly.

Note that claim 50 does not require the 1st and 2nd regions both physically/electrically contact with the same source (or both physically/electrically contact with the same drain).

Claim 60 does not require the 3rd and 4th regions physically/electrically contact with another pair of source/drain. Shimizu, in figs. 9E, discloses first and second n-type regions 31 are electrically in contact with the same pair of the p-type source and drain regions.

FIG. 9E



Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 40-42 and 51-53 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Shimizu (US Pat. 5,217,910).

Shimizu discloses a but fails to disclose the concentration of the first, second impurity region is about 1×10^{17} to 5×10^{19} atoms/cm³ (claims 40 and 51); the width of first, second impurity regions along boundary is 0.05 to 0.3 μ m (claims 41 and 52); the interval between first and second impurity regions is 0.04 to 0.6 μ m (claims 42 and 53). It appears that having a specific width/ interval and concentration of the impurity regions as claimed is *prima facie* obvious due to the fact that one can vary the width/ interval and concentration of the impurity

regions in order to achieve a specific MOSFET device. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined process of Shimizu in view of Sanchez by selecting a suitable the width/ interval and concentration, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). Moreover, as the width/ interval and concentration of the impurity regions does seem to be critical to the invention, it must be shown that any one or all of the listed materials yield an unexpected product or result. *In re Margolis* 228 USPQ 940 (Fed. Cir. 1986); *In re Kirsch* 182 USPQ 286 (CCPA 1974); *In re Suether* 181 USPQ 36 (CCPA 1974); *In re Costello* 178 USPQ 290 (CCPA 1973); *In re Von Schickh* 150 USPQ 300 (CCPA 1966); *In re Sussman* 60 USPQ 538 (CCPA 1944); *In re Kaplan* 45 USPQ 175 (CCPA 1940).

3. Claims 54-58 and 61 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Shimizu (US Pat. 5,217,910) in view of Sanchez (US Pat. 5,583,067).

Regarding claims 54, 55 and 61, Shimizu discloses in figs. 9E a semiconductor device comprising:

a semiconductor substrate 21;

a channel region formed in semiconductor substrate 21; wherein channel region is located between p-source and p-drain regions;

at least first and second impurity regions 31 formed in channel region wherein first impurity region 31 (on the left side of the gate) is **electrically** in contact with the p-source region

(left p-region) and second impurity region 31 (on the right side of the gate) is **electrically** in contact with the p-drain region (right p-region); first and second impurity regions 31 (n-type) are doped with an impurity of a conductivity type opposite to source and drain regions (p-type); wherein first (left side) and second (right side) impurity regions are separated from each other; in other word, the first and second impurity regions 31 are in contact with the same pair of p-source/drain.

at least third and fourth impurity regions 37 (n⁻-doped regions) formed in semiconductor substrate wherein third impurity regions 37 (right n-region 37) are **electrically** in contact with the drain regions (right p-region) and fourth impurity regions 37 (left n-region 37) are **electrically** in contact with the source regions (left p-region)

a gate insulating film formed over the channel region; and

a gate electrode 28 over the channel region with the gate insulating film interposed therebetween, wherein first (left side) and second (right side) impurity regions are separated from each other; and wherein first and second impurity regions 31 are overlapped by gate electrode at least partly.

Note that claim 54 does not require the 1st and 2nd regions both physically/electrically contact with the same source (or both physically/electrically contact with the same drain). Claim 61 does not require the 3rd and 4th regions physically/electrically contact with another pair of source/drain. Shimizu, in figs. 9E, discloses first and second n-type regions 31 are electrically in contact with the same pair of the p-type source and drain regions.

Shimizu discloses a semiconductor device as describe above but fails to disclose the metal silicide is formed on the source /drain surface. However, Sanchez teaches a similar gate structures having the silicide regions 21a/b form over the source/drain regions 20a/b (fig. 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Shimizu by forming the silicide regions as taught by Sanchez in order to form a low resistivity upper surface regions.

Regarding claims 56-58, the combination of Shimizu and Sanchez also fails to disclose the concentration of the first, second impurity region is about 1×10^{17} to 5×10^{19} atoms/cm³ (claim 56); the width of first, second impurity regions along boundary is 0.05 to 0.3 μm (claim 57); the interval between first and second impurity regions is 0.04 to 0.6 μm (claim 58). It appears that having a specific width/ interval and concentration of the impurity regions as claimed is *prima facie* obvious due to the fact that one can vary the width/ interval and concentration of the impurity regions in order to achieve a specific MOSFET device. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined process of Shimizu in view of Sanchez by selecting a suitable the width/ interval and concentration, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). Moreover, as the width/ interval and concentration of the impurity regions does seem to be critical to the invention, it must be shown that any one or all of the listed materials yield an unexpected product or result. *In re Margolis* 228 USPQ 940 (Fed. Cir. 1986); *In re Kirsch* 182 USPQ 286 (CCPA 1974); *In re*

Suether 181 USPQ 36 (CCPA 1974); *In re Costello* 178 USPQ 290 (CCPA 1973); *In re Von Schickh* 150 USPQ 300 (CCPA 1966); *In re Sussman* 60 USPQ 538 (CCPA 1944); *In re Kaplan* 45 USPQ 175 (CCPA 1940).

Allowable Subject Matter

4. Claims 43-49 are allowed.

The following is an examiner's statement of reason for allowance: the prior art of record, either singularly or in combination, does not disclose or suggest a semiconductor device comprising: at least first and second impurity regions formed in said channel region, wherein said first and second impurity regions are in contact with the source region and are separated from each other; at least third and fourth impurity regions formed in said semiconductor channel wherein third and fourth impurity regions are in contact with the drain region and are separated from each other; wherein each of said first, second, third and fourth impurity regions is doped with an impurity of a conductivity type opposite to that of said source and drain regions.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

5. Applicant's arguments with respect to claims 39-61 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (571) 272-1798. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke H can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/DAVID VU/

Primary Examiner, Art Unit 2818